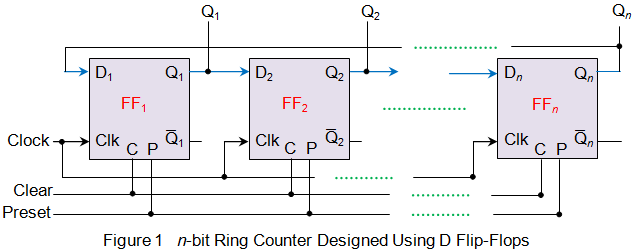


**Figure 1. An n-bit Parallel-In Serial-Out Left-Shift Register. In PISO shift registers, the data is loaded into the register in parallel format while it is retrieved from it serially.**



**Figure 2. An n-bit Ring Counter**

**module PISO\_LSHIFT (CLK, CLR, SHL, DIN, Q);**

**input CLK, CLR, SHL;**

**input [7:0] DIN;**

**output Q;**

**reg Q;**

**reg [7:0] SHIFTER;**

**always @ (posedge CLK)**

**if (CLR)**

**SHIFTER = 8'b0;**

**else**

**if (~SHL)**

**SHIFTER = DIN;**

**else**

**begin**

**Q = SHIFTER[7];**

**SHIFTER = {SHIFTER[6:0], 1'b0};**

**end**

**endmodule**

**module test\_PISO\_LSHIFT;**

**reg CLK, CLR, SHL;**

**reg [7:0] DIN;**

**wire Q;**

**PISO\_LSHIFT s1 (CLK, CLR, SHL, DIN, Q);**

**always**

**#5 CLK = ~CLK;**

**initial**

**begin**

**CLK = 1'b0;**

**CLR = 1'b1;**

**DIN = 8'b10101101;**

**#10 CLR = 1'b0;**

**#5 SHL = 1'b0;**

**#6 SHL = 1'b1;**

**end**

**endmodule**